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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/471,637
Filing Date	December 23, 1999
First Named Inventor	Yuval Bachrach
Art Unit	2131
Examiner Name	Christian A. LaForgia
Total Number of Pages in This Submission: 38	Attorney Docket Number: 42390.P7286

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form (2 copies)
- [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [ ] After Allowance communication to Technology Center (TC)
- [x] Appeal Communication to Board of Appeals and Interferences **
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- [ ] Proprietary Information
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- [ ] Other Enclosure(s) (please Identify below):

Remarks

** Appeal Brief in triplicate is enclosed.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	John Patrick Ward, Reg. No. 40,216
Signature	
Date	April 28, 2004

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AFF/2131

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/471,637
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METHOD OF PAYMENT *(check all that apply)*

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X	=
Independent Claims		-3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	John Patrick Ward	*Registration No. (Attorney/Agent)*	40,216	*Telephone*	408-720-8300
Signature				*Date*	April 28, 2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	**09/471,637**
Applicant	:	**Bachrach, Y.**
Filed	:	**12/23/1999**
TC/AU	:	**2131**
Examiner	:	**Laforgia, C. A.**
Docket No.	:	**p7286**

Confirmation No. **7753**

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on April 28, 2004
Date of Deposit

Anne Collette
Name of Person Mailing Correspondence

Anne Collette 4/28/2004
Signature Date

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Appeal Brief under 37 C.F.R. §1.192

Commissioner for Patents:

The applicant ("Applicant") respectfully submits this Brief in triplicate in support of his appeal from a final decision by the Examiner in the above-identified case.

An oral hearing is not desired.

1. Real Party of Interest

Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052, is the assignee of the present invention and the real party of interest.

2. Related Appeals and Interferences

To the best of Applicants' knowledge, there are no appeals or interferences related to the present Appeal which will directly affect, be directly affected by, or have a bearing on the Board's decision.

3. Status of the Claims

Claims 1-21 are presently active.

Claims 1, 2, 8, 9, 15, and 16 stand rejected under 35 U.S.C. §102(e) as being anticipated by Boucher, et al., US patent 6,427,173 ("Boucher"); claims 3, 4, and 6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Boucher in view of Rubin, US patent 4,525,795 ("Rubin"); and claims 5, 7, 10-14, and 17-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Boucher in view of Findlater, et al., U.S. patent 6,385,208 ("Findlater").

4. Status of Amendments

No amendment has been filed subsequent to the final rejection.

5. Summary of the Invention

The present invention is directed to a network interface device comprising a PHY (Physical Layer) and a MAC (Media Access Control Layer). The PHY and MAC layers communicate with each other. The communication between the PHY and the MAC is in the form of PHY-to-MAC words and MAC-to-PHY words. A PHY-to-MAC word is a word that is sent by the PHY to the MAC, and a MAC-to-PHY word is a word that is sent by the MAC to the PHY. A word may contain data, control information, or both.

Embodiments of the present invention provide a flexible communication interface between the MAC and the PHY so that many data speeds for exchanging information between the PHY and the MAC may be realized in a flexible manner without changing the clock signal frequency. This is accomplished by using information in a word format, where the word format supports a slow-mode PHY-to-MAC word. More specifically, a PHY-to-MAC word has a transmit cycle field. When a PHY-to-MAC word is received by the MAC, the MAC may or may not provide data to the PHY in the "next" MAC-to-PHY word, depending upon whether the transmit cycle field in the PHY-to-MAC word is a 1 or 0.

Loosely stated, the transmit cycle field controls the "flow" of data sent by the MAC to the PHY. If the transmit cycle field in a PHY-to-MAC word is such that the MAC is instructed not to send data in a next MAC-to-PHY word, then this flow of data is effectively decreased. By allowing for the PHY to instruct the MAC when to send data in a next MAC-to-PHY word, many data speeds may be handled in a flexible manner.

6. Issue

Whether claims 1, 2, 8, 9, 15, and 16 stand rejected under 35 U.S.C. §102(e) as being anticipated by Boucher, et al., US patent 6,427,173 ("Boucher"); whether claims 3, 4, and 6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Boucher in view of Rubin, US patent 4,525,795 ("Rubin"); and whether claims 5, 7, 10-14, and 17-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Boucher in view of Findlater, et al., U.S. patent 6,385,208 ("Findlater").

7. Grouping of Claims

Applicants assert that all of the claims at issue fall into one group.

All of the claims recite the limitation that the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word. Consequently, for purposes of this appeal, all of the claims fall into one group.

8. Argument

In the final office action mailed 12 November 2003 ("Office Action"), claims 1, 2, 8, 9, 15, and 16 were rejected under 35 U.S.C. §102(e) as being anticipated by Boucher. Specifically, beginning at the top of page 4 of the Office Action, it is stated that Boucher teaches the claim limitation that the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word. In support of this assertion, the Office Action makes reference to Boucher, figures 4B, 4D, 6, 9, and 22, as well as column 8, lines 28-63; column 9, lines 13-66; column 10, lines 18-34; column 11, lines 22-46; and column 17, lines 9-34.

Boucher does not teach this claim limitation. Boucher teaches how the processing of received data packets may be accelerated, where messages selected for "fast-path" processing avoid the standard protocol stack and instead are handled by special purpose hardware. Boucher does not teach that communication between a MAC and a PHY is word based, and more particularly, Boucher does not teach a word based interface between a MAC and a PHY where a slow mode PHY-to-MAC word has a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

Furthermore, Applicant respectfully believes that the argument in the Office Action, item number 6, pages 2-3, incorrectly considers communication of the PHY over the medium as somehow anticipating the present invention. For example, near the top of page 3 of the Office Action, it is stated that "the MAC is responsible for informing the PHY which speed the data will be received at, i.e. 10Base-T, 10Base-T2, etc." However, the present invention is directed to how a MAC and a PHY communicate with each other via a word based interface. The present invention is not directly concerned with how a PHY communicates with another PHY over a medium.

By allowing for a flexible word based interface between a PHY and a MAC, it is possible for a MAC to be used with various types of PHYs from perhaps different manufacturers. In some instances, the MAC may be able to transfer data to a PHY faster than the PHY is able to transmit data on the medium. In such a case, a slow mode is used whereby not all words transmitted from the MAC to the PHY contain data to be transmitted over the medium. In this way, various data link speeds may be supported without changing the clock signal frequency between the MAC and the PHY. (See page 5, lines 13-20, and page 6, lines 5-13 of the present application.) This is the motivation for the present invention. This practical feature is realized by inventions defined by the present claims, specifically, the claim limitation reciting a slow mode PHY-to-MAC word, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

In the Office Action, claims 3, 4, and 6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Boucher in view of Rubin. However, Rubin is cited merely for teaching words that are each 12 bits wide. Consequently, for the reasons given above regarding Boucher, claims 3, 4, and 6 are believed patentable over Boucher and Rubin.

In the Office Action, claims 5, 7, 10-14, and 17-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Boucher in view of Findlater. In the Office Action, page 9, Findlater is cited for merely teaching PHY-to-MAC words that have data fields in various bit positions. But Applicant asserts that nowhere does Findlater teach a word based interface, and more particularly, nowhere does Findlater teach or suggest the claimed limitation of a slow mode PHY-to-MAC word that includes a transmit cycle filed to indicate whether the MAC is to provide data in the next MAC-to-PHY word. Consequently, for the reasons given above regarding Boucher, claims 5, 7, 10-14, and 17-21 are believed patentable over Boucher in view of Findlater.

Conclusion

For the above reasons, the Board is respectfully requested to vacate the Examiner's rejection of the pending claims, to remand this application to the Examiner, and to direct the Examiner to pass this case to issuance.

Respectfully submitted,

Seth Z. Kalson Dated: 4-26-04

Seth Z. Kalson
Reg. no. 40,670
Attorney for Applicants and Intel Corporation (Assignee)

9. Appendix

1. (Previously Presented) A MAC comprising:

at least one PHY-to-MAC port to receive signals indicative of PHY-to-MAC words; and

at least one MAC-to-PHY port to transmit signals indicative of MAC-to-PHY words;

wherein the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word received by the MAC from a PHY includes a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

2. (Previously Presented) The MAC as set forth in claim 1, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word received by the MAC from the PHY indicates that the MAC is to provide data in the next MAC-to-PHY word.

3. (Original) The MAC as set forth in claim 1, wherein the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

4. (Original) The MAC as set forth in claim 1, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

5. (Original) The MAC as set forth in claim 4, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

6. (Previously Presented) The MAC as set forth in claim 4, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word received by the MAC from the PHY indicates that the MAC is to provide data in the next MAC-to-PHY word; and

the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

7. (Original) The MAC as set forth in claim 6, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.

8. (Previously Presented) A PHY to transmit and receive signals propagated on a medium, and to communicate with a MAC via PHY-to-MAC words and MAC-to-PHY words, the PHY comprising:

at least one MAC-to-PHY port to receive signals indicative of the MAC-to-PHY words; and

at least one PHY-to-MAC port to transmit signals indicative of the PHY-to-MAC words; wherein the PHY-to-MAC words include slow mode PHY-to-MAC words, wherein a slow mode PHY-to-MAC word transmitted by the PHY and received by the MAC includes a transmit cycle field to indicate whether the MAC is requested by the PHY to provide data for transmission on the medium in a next MAC-to-PHY word transmitted by the MAC to the PHY subsequent to the MAC receiving the slow mode PHY-to-MAC word.

9. (Previously Presented) The PHY as set forth in claim 8, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word transmitted by the PHY to the MAC indicates that the MAC is to provide data in the next MAC-to-PHY word.

10. (Original) The PHY as set forth in claim 8, wherein the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

11. (Original) The PHY as set forth in claim 8, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

12. (Original) The PHY as set forth in claim 11, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

13. (Previously Presented) The PHY as set forth in claim 11, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words, wherein an equal speed mode PHY-to-MAC word transmitted by the PHY to the MAC indicates that the MAC is to provide data in the next MAC-to-PHY word; and

the PHY-to-MAC words and MAC-to-PHY words are each 12 bits wide.

14. (Original) The PHY as set forth in claim 13, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.

15. (Previously Presented) A computer system comprising:

a MAC; and

a PHY to receive and transmit signals propagated on a medium and connected to the MAC so that the MAC provides MAC-to-PHY words to the PHY and the PHY provides PHY-to-MAC words to the MAC;

wherein the PHY-to-MAC words and the MAC-to-PHY words are synchronously paired so that the MAC provides one MAC-to-PHY word to the PHY while the PHY provides one PHY-to-MAC word to the MAC;

wherein the PHY-to-MAC words include slow mode PHY-to-MAC words having a transmit cycle field;

wherein if the transmit cycle field of a first slow mode PHY-to-MAC word is set to a first value, the first slow mode PHY-to-MAC word being synchronously paired with a first MAC-to-PHY word, then the MAC is requested by the PHY to provide transmit data in a second MAC-to-PHY word for transmission over the medium, where the second MAC-to-PHY word succeeds the first MAC-to-PHY word, and if the transmit cycle field of the first slow mode PHY-to-MAC word is set to a second value different from the first value, then the MAC is requested by the PHY not to include transmit data in the second MAC-to-PHY word.

16. (Original) The computer system as set forth in claim 15, wherein the PHY-to-MAC words include equal speed mode PHY-to-MAC words.

17. (Original) The computer system as set forth in claim 15, wherein the PHY-to-MAC words and MAC-to-PHY words are 12 bits wide.

18. (Original) The computer system as set forth in claim 15, wherein the transmit cycle field is in bit position nine, counting from zero, of a slow mode PHY-to-MAC word.

19. (Original) The computer system as set forth in claim 18, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven.

20. (Original) The computer system as set forth in claim 18, wherein

the PHY-to-MAC words include equal speed mode PHY-to-MAC words; and

the PHY-to-MAC words and MAC-to-PHY words are 12 bits wide.

21. (Original) The computer system as set forth in claim 20, wherein

the slow mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit position three, a receive cycle field in bit position ten, and a receive data valid field in bit position eleven; and

the equal speed mode PHY-to-MAC words have receive data fields in bit positions zero, one, two, four, five, six, seven, and eight, a carrier sense signal field in bit

position three, a receive cycle field in bit position ten, a receive data valid field in bit position eleven, and a management frames protocol data out field in bit position nine.